Claim Rejections

Claims 1, 2-4, 7, 11-15, 17, 21, 24-28, 39-43, 45-47, 49-51, and 54 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Lattibeaudiere in view of Abbott. Applicants submit that claim 1 is patentable over the cited references.

Claim 1 recites, in part:

> receiving an input data having a plurality of bit groups, wherein **a first bit group** has a first position in the input data relative to other bit groups, wherein the input data has **a second bit group** having a second position in the input data relative to other bit groups;
>
> **translating**, in response to first translation information, **the first bit group** from the first position to a different position **in a comparand**;
>
> **translating** the **second bit group** from the second position to a second position **of the comparand** in response to second translation information

(emphasis added)

In regards to claim 1, the Office Action states, in part:

> In regard to claim 1, Lattibeaudiere teaches: "a method of operating a content addressable memory (CAM) device, comprising:" (e.g., see column 4 lines 15-20) "comparing the comparand with data stored in a CAM array" (e.g., see column 17 lines 67-68, column 18 lines 1-6). Comparand or search/key data is the input data to be compared/matched with the stored data in the CAM. This data is often stored in a Comparand or search/key register at the input of a CAM device. "receiving an input data having a plurality of bit group," (e.g., see column 3 lines 32-40, Figures 2a-2c) "wherein a first bit group has a first position in the input data relative to the other bit group," (e.g., see paragraph 3 lines 32-40, paragraph 5 lines 60-66, and Figures. 2a-2c). For example DATA_WRITE_CMD field (bits 24-31) in Figure 2a. "wherein the input data has a second bit group having second position in the input data relative to the other bit group;" (e.g., see paragraph 4 lines 20-26, paragraph 5 lines 60-66, and Figures. 2a-2c). For example CAM_ADDR field in Figure 2a.

(Office Action 2/6/04, p. 2-3)(underlining emphasis added)

Applicant respectfully disagrees with the Office Action's characterization of the cited references. First, applicants submit that there is no motivation to combine the

references in the manner purported by the Office Action. In particular, the Office Action states

> Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine in the Contend Addressable Memory system of Lattibeaudiere with the circuits taught by Abbott. The modification would have provided dynamic programmability in performing a number of logical operations (e.g., see abstract). It is understood by those skilled in art that Programmable Logics Devices (PLDs) are often used to implement various circuit functions during design and proto typing. The programmability feature of these devices, gives the designer the flexibility to test and verify their design before committing to manufacturing, which in turn reduces the cost and time involved with repeated manufacturing processes

(Office Action 2/6/04, p. 4)(underlining emphasis added)

It is respectfully submitted that the Office Action has not provided a motivation to combine references. The Office Action has merely stated the function of a PLD: that of providing dynamic programmability in performing logic operations. Such is not a motivation as to why one of skill in the art, confronted with the same problems as the inventor of Lattibeaudiere, and with no knowledge of applicants' claimed invention, would be motivated to combine the references in the purported by the Office Action. It is submitted that the Office Action must provide "a specific understanding or principle within the knowledge of the skilled artisan" that would have provided the motivation to combine the references in the purported manner. See MPEP 2143.01; In re Kotzab, 217 F.3d 1365 (Fed. Cir. 2000). The purported "understanding" provided by the Office Action merely explains the use of PLDs and does not provide a specific principle that would have provided a motivate to combine the PLD teachings of Abbott with the CAM of Lattibeaudiere.

Moreover, applicants submit that if even one were to somehow combine the reference as purported by the Office Action, such a combination would still lack at least one limitation appearing in claim 1. In particular, it appears that the Office Action is reading the first and second bit groups of claim 1 onto the DATA_WRITE_CMD field

and CAM_ADDR field of Lattibeaudiere. (Office Action 2/6/04, p. 3). The DATA_WRITE_CMD and CAM_ADDR fields of Lattibeaudiere are **command fields** that are only used to control the operation of the memory system. These command fields are **not stored in the CAM and not used to form the comparand**. (Lattibeaudiere, col. 5, lines 9-25). Therefore, there would be no reason to "translate" these command fields to a comparand, regardless of their bit positions.

In contrast, the first and second bit groups of claim 1 are translated to a comparand. Therefore, applicants submit that claim 1 is patentable over the cited references.

Given that claims 2-4, 7, 11-13 depend from claim 1, applicants submit that claims 2-4, 7, 11-13 are also patentable over the cited references.

For reasons similar to those given above with respect to claim 1, applicants submit that claims 15, 17, 21, 24-28, 29, 39-43, 45-47, 49-51 and 54 are patentable over the cited references.

Claims 29, 33-34 and 37 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Miller in view of Abbott. It is submitted that claims 29, 33-34 and 37 are patentable over the cited references.

The Office Action states in part:

> Abbott however teaches "a plurality of translation circuitry, each of the plurality of translation circuitry coupled to corresponding one of the plurality of CAM blocks, (e.g., see column 7 lines 6-15 and 26-30). It should be understood by those skilled in art that while one rearrangement (translation) circuitry shown in the reference, it can be adapted to make as many circuits as is desired by using the same or additional PLDs. . .
>
> "the output coupled to transmit the comparand to the CAM block," (e.g. the output of rearrangement circuitry in PLD is connected to the input of each CAM block).
>
> The PLDs can be configured to perform one or more of a variety of application. Furthermore, the one or more function may be dynamically

> (e.g., on a cycle-by-cycle basis) programmed into the PLD (column 17 lines 5-10). As an example, the reference implements a CAM function using the PLD. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the CAM blocks of Miller et al to the rearrangement (translation) circuits taught by Abbott. The modification would have provided dynamic programmability in performing a number of logical operations (e.g., see abstract). It is understood by those skilled in art that Programmable Logics Devices are often used to implement various circuit functions during design and proto typing. The programmability feature of these devices, gives the designers the flexibility to test and verify their design before committing to manufacturing, which in turn reduces the cost and time involved with repeated manufacturing processes.

(Office Action 2/6/04, p. 18-19)

It is respectfully submitted that the Office Action has not provided a motivation to combine references. The Office Action has merely stated the function of a PLD: that of providing dynamic programmability in performing logic operations. Such is not a motivation as to why one of skill in the art, confronted with the same problems as the inventors of Miller, and with no knowledge of applicants' claimed invention, would be motivated to combine the references in the purported by the Office Action. It is submitted that the Office Action must provide "a specific understanding or principle within the knowledge of the skilled artisan" that would have provided the motivation to combine the references in the purported manner. See MPEP 2143.01; In re Kotzab, 217 F.3d 1365 (Fed. Cir. 2000). The purported "understanding" provided by the Office Action merely explains the use of PLDs and does not provide a specific principle that would have provided a motivate to combine the PLD teachings of Abbott with the CAM of Miller.

The Office Action purports that the one of skill in the art would connect the output of the rearrangement circuitry in the PLD of Abbott to the input of each of the CAM blocks in Miller but provides no understanding or principle as to why one of skill in the art would be motivated to modify Miller in this manner. Moreover,

applicants submit that there is no motivation to modify Miller in such a manner. The problem confronting the inventors of Miller was the reallocation of CAM sub-arrays to process different length CIDR prefixes. To solve this problem, Miller teaches methods of processing CIDR addresses having variable prefix lengths by generating a hit signal and an index signal with each of the CAM blocks in response to a CIDR address. **Miller is completely devoid of any teaching with respect to the receipt of input data and generation of a corresponding comparand. Therefore, it is submit that one of skill in the art facing the problems confronting the inventors of Miller would not look to the teachings Abbott for solutions to their problem.** It is respectfully submitted that applicants' own disclosure cannot be used to provide a motivation for combining references.

Furthermore, applicants submit that there can be no combination of references to render a claim obvious where the suggested combination of references would require a substantial reconstruction and redesign of the elements shown in the Miller as well as a change in the basic principle under which the CAM of Miller was designed to operate. In re Rattie, 270 F.2d 810 (CCPA 1959); MPEP 2143.01. The suggested modification of Miller with the rearrangement circuitry of Abbott would not only require substantial redesign of Miller but would also substantially redesign Miller without any explained or understood purpose for doing so in Miller.

Therefore, applicants submit that claims 29, 33-34 and 37 are patentable over the cited references.

Claims 56-60 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Feldmeier in view of Abbott. It is submitted that claims 56-60 are patentable over the cited references.

Claim 56 recites:

An apparatus, comprising:

a content addressable memory (CAM) array to receive a comparand; and

a translation circuitry having at least one first input, at least one second input, and at least one output, wherein the first input is configured to receive an input data having a plurality of bit groups, wherein a first bit group has a first position in the input data relative to other bit groups, **wherein the second input is configured to receive translation information indicative of translation of the first bit group from the first position to a different position in a comparand,** the output coupled to the CAM array to transmit the comparand to the CAM array, **wherein the translation circuitry comprises a switch circuit having at least one demultiplexer.**

(emphasis added)

The Office Action states:

> In regard to claim 46, Feldmeier teaches: "An apparatus comprising: a content addressable memory (CAM) array to receive a comparand" (e.g., see paragraph 22 in page 16) "the output coupled to the CAM array to transmit the comparand to the CAM array," (e.g., see abstract, paragraph 22 in page 16) "wherein the translation circuitry comprises a switch having at least one demultiplexer" (e.g., see paragraph 30 in page 18, element 1620 in Figure 16) but does not teach: "a translation circuitry having at least one first input, at least one second input, and at least one output, wherein the first input is configured to receive an input data having the plurality of bit groups, wherein a first bit group has a first position in the input data relative to other bit groups, wherein the second input is configured to receive the translation information indicative of translation of the first bit group from the first position to a different position in a comparand;"

(Office Action 2/6/04, p. 20-21)

It is not understood which parts of Feldmeier the examiner is rely on for support of its teaching assertions. The cited Feldmeier reference is a U.S. Patent 5,920,886 having column and line numbers. The Office Action cites to some unknown paragraph and page numbers. Although the reference citations for the rejection in the Office Action is unclear, applicants are herewith making a response as best as possible in an attempt to advance prosecution of this case. If, however, the Examiner continues to advocate the unpatentability of any of the claims in this application, then the Examiner is respectfully

requested to specifically designate the particular part of a reference relied on in making a rejection with pertinant citations.

It appears that the Office Action is attempting to read the claimed "translation circuitry" on the demultiplexer of Feldmeier. Applicants submit that such a reading is inapposite. Feldmeier teaches that demultiplexer 1330 routes a packet receive from input packet queue 1310 to one of output packet queues 1350, 1360 or 1370 depending on the signal received from IP address lookup 1340. (Feldmeier, col. 13, lines 1-5; Figure 13). It is respectfully submitted that the routing of packet does not involve any translation of bits in the packet.

Furthermore, the address "translation" of Feldmeier refers to the conversion of a ternary address into two or more binary addresses. While hierarchical addresses can be directly stored in ternary CAMs, in order to be stored in binary CAMs they must first be converted into binary format. Binary CAMs store binary entries, while ternary CAMs store ternary entries. Binary entries are entries that contain only 0 or 1 values, while ternary entries are entries that contain 0, 1 or X (i.e., "don't care") values. A single ternary entry can be expressed as two or more binary entries. In other words, a single ternary entry "1X0" can be represented by two binary entries "110" and "100", or a single ternary entry "1XX" can be represented by four binary entries "100", "101", "110" and "111", etc. As hierarchical addresses often comprise ternary values (e.g. "908-979-XXXX"), ternary CAMs require a smaller number of table entries to represent each hierarchical address than binary CAMs. For example, ternary address "908-979-XXXX" would be converted into 10,000 binary addresses, "908-979-0000" through "908-979-9999." (Feldmeier, columns 3 and 4).

Nothing in Feldmeier, either alone or in combination with Abbot, teaches or suggests translation of the first bit group from a first position to a different position in a comparand. In contrast, claim 56 includes the limitation that the translation circuitry,

comprising a switch circuit having a least one demultiplexer, receives translation information indicative of translation of the first bit group from the first position to a different position in a comparand.

It is also respectfully submitted that the Office Action has not provided a motivation to combine references. The Office Action has merely stated the function of a PLD: that of providing dynamic programmability in performing logic operations. Furthermore, applicants submit that there can be no combination of references to render a claim obvious where the suggested combination of references would require a substantial reconstruction and redesign of the elements shown in the Feldmeier as well as a change in the basic principle under which the CAM of Feldmeier was designed to operate. In re Rattie, 270 F.2d 810 (CCPA 1959); MPEP 2143.01. The suggested modification of Feldmeier with the rearrangement circuitry of Abbott would not only require substantial redesign of Miller but would also substantially redesign Feldmeier without any explained or understood purpose for doing so in Feldmeier.

Therefore, applicants submit that claims 56-60 are patentable over the cited references.

In conclusion, applicants respectfully submit that in view of the arguments set forth herein, the applicable rejections have been overcome.

If the Examiner believes a telephone interview would expedite the prosecution of this application, the Examiner is invited to contact Daniel Ovanezian at (408) 720-8300.

If there are any additional charges, please charge our Deposit Account No. 02-2666.

Respectfully submitted,

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Dated: 6/9, 2004

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